AGP/DDR INTERFACES FOR FULL SWING AND REDUCED SWING (SSTL) SIGNALS ON AN INTEGRATED CIRCUIT CHIP

ABSTRACT OF THE DISCLOSURE

An I/O interface includes latches, clocks, and conditioning circuits implemented in a custom physical layout to produce a reliable and flexible interface to high frequency busses running a plurality of protocols and signal specifications. Three clock trees are used to synchronize the buffering and conditioning of input/output signals before sending such signals to a pad or core. The clock trees are implemented via custom layouts to allow tight control of clock/strobe parameters (e.g., skew, duty cycle, rise/fall times). Two of the clock trees are local to the I/O interface and trigger a plurality of output latches configured on-the-fly to buffer output data signals from the core in asynchronous or synchronous mode. In the synchronous mode, a clock/strobe could be either edge-centered or window-strobe with respect to the data. The third clock tree distributes clock/strobes from an external source and is used to trigger a plurality of input latches configured on-the-fly to buffer input data from the pad in either a window-strobe mode or an edge-centered mode. The I/O interface also includes conditioning circuits that condition the I/O signals to be compliant with AGP/DDR protocols, as well as, full swing, reduced swing (SSTL), and TTL signal specifications.